REMARKS

Applicants acknowledge receipt of the Examiner's Advisory Action dated November 12, 2003. Applicants respectfully request entry of the amendments originally presented in the response mailed Dec. 1, 2003.

Claims 1-4, 6, 7, 9-11 and 14-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ishikawa, U.S. Patent No. 5,748,018. Applicants respectfully traverse this rejection.

The Examiner contends that Ishikawa teaches "a register having a first input for receiving a data signal, a second input for receiving a clock signal, and an output; and a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register", as recited in claim 1. In particular, the Examiner states that D-FF (D-Flip Flop) 101 and buffer 103 of Ishikawa respectively teach the register and buffer recited in claim 1. Office Action, pp. 2-3.

At col. 4, lines 14-33, Ishikawa recites:

> Referring to FIG. 2B, there is shown a timing chart illustrating an operation of the data output circuit shown in FIG. 2A. In addition, "assuming that an internal delay time of the D-FF 101 as compared with the external clock signal CLK is t_q, and a delay time of the output buffer 102 as compared with the output of the D-FF 101 is t_b, a delay time t_d in the data transfer as compared with the external clock CLK is expressed as $t_q + t_b$. On the other hand, assuming that a difference in time between the external clock signal CLK and the delayed clock signal CLKD is t_b, a delay time t_D in the data transfer as compared with the delayed clock CLKD is expressed as follows:
>
> $t_D = t_q + t_b - t_b = t_q$
>
> Accordingly, the delay time t_D in the data transfer becomes equal to t_q, and therefore, this becomes substantially equivalent to the fact that the internal clock signal is advanced as compared with the external clock by the time t_b by using the PLL circuit.

Ishikawa also teaches that the data transfer can be executed within Tcycle "if the delay time t_{B103} of the output buffer 103 is set to a value not smaller than $\{t_s + t_q + t_b - Tcycle\}$". Ishikawa, col. 5, lines 14-28. Ishikawa neither teaches nor suggests making the

delay of buffer 103 (which the Examiner relies on to teach the "buffer" of claim 1) substantially equivalent to the delay of D-FF 101 (which the Examiner relies on to teach the "register" of claim 1).

In the Advisory Action mailed January 22, 2004, the Examiner also relies on FIG. 2B of Ishikawa to disclose "a timing diagram, in which the buffer generating a delay Tb that's substantially equivalent or equal to the delay through said register Tq." As stated in Ishikawa, FIG. 2B is based on the assumptions that "an internal delay time of the D-FF 101 as compared with the external clock signal CLK is tq, and a delay time of the output buffer 102 as compared with the output of the D-FF 101 is tb." Ishikawa, col. 4, lines 16-19. Thus, the time tb shown in FIG. 2B is the delay of output buffer 102, not the delay of output buffer 103. As shown in FIG. 2A, buffer 102 is coupled to the output of the D-FF. Buffer 102 is clearly not coupled to receive a clock signal. Throughout the rest of the rejection, the Examiner relies on output buffer 103 to anticipate the buffer of Applicants' claim 1. No teaching or suggestion that the delay of buffer 103 is equal to the delay of buffer 102 has been provided. Accordingly, FIG. 2B fails to anticipate claim 1.

Furthermore, even assuming for the sake of argument that the delay of output buffer 102 is the same as the delay of output buffer 103, it is not clear how FIG. 2B teaches a buffer with a delay equal to the delay of a register. In FIG. 2B, the quantity tq+tb appears to be more than twice the length of tb, suggesting that tb and tq are not equal. Additionally, the timing diagram of FIG. 2B is not drawn to any particular scale, and thus one of ordinary skill in the art could easily interpret any apparent correlation between tq and tb as a coincidence, especially given that none of the cited portions of the reference suggest such a relationship between these two quantities.

Further with respect to claim 1, Applicant notes that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). The cited art fails to teach or suggest "a source clock domain in a first network protocol layer" and "a destination clock domain in a second network protocol layer", as recited in claim 1. The Examiner cites the data output circuit 100 of FIG. 3A of Ishikawa as being "a first layer" and the data input circuit 200 in the same figure as being "a

second layer." However, these circuits are clearly not implementing network protocol layers (in fact, none of the terms "network", "layer", or "protocol" are used in Ishikawa). Since these features of claim 1 are neither taught nor suggested in the cited art, Applicant requests the withdrawal of this rejection.

Applicant requests the withdrawal of the rejection of claims 2-4, 6, 7, 9-11 and 14-19 for reasons similar to those provided above with respect to claim 1.

Additionally with respect to claim 2, Applicant notes that: "In relying on a theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The Examiner states that "the implementation of link layer and physical layer is inherent in the interconnection between the various components of the integrated circuit shown in FIG. 3A". Office Action, p. 3. However, the interconnection of the various components shown in FIG. 3A could arise in a variety of environments, such as an interface between integrated circuits (e.g., a processor and memory) on a mother board in a computer system, that do not implement a link layer and a physical layer. Since the implementation of a link layer and a physical layer is not necessary to implement the circuit shown in FIG. 3A, a link layer and a physical layer are clearly not inherent in FIG. 3A. Accordingly, Applicant requests the withdrawal of this rejection.

Similarly, with respect to claim 4, Applicant notes that there is no basis for the Examiner's assertion that "Ishikawa discloses a delay circuit (implicitly shown) between said source clock domain and said destination clock domain". Office Action, p. 4. The Examiner cites a portion of Ishikawa that describes an "output buffer 103 having an input connected to the clock terminal 104 to receive the external clock CLK and an output connected to a clock output terminal 105 for outputting a delayed clock CLKD which is delayed from the external clock signal CLK by a delay time of the output buffer 103." Ishikawa, col. 4, lines 8-13. This statement, which merely describes the operation of buffer 103, clearly fails to imply the existence of a delay circuit. Since the cited art fails to teach or suggest "a delay circuit, coupled between said source clock domain and said

destination clock domain," as recited in claim 4, Applicant requests that this rejection be withdrawn.

Additionally with respect to claim 9, the cited art fails to teach or suggest "receiving an input clock signal in a first clock domain in a first layer; receiving an input data signal in the first clock domain in the first layer; latching the input data signal by triggering the input data signal by the input clock signal; [and] delaying the input clock signal by an amount that is equal to the delay in the latching", as recited in claim 9 (emphasis added). Applicant notes that this claim recites that the input clock signal is delayed by an amount that is equal to the delay in the latching. Given the above reasons why the cited art fails to teach a buffer generating a delay that is substantially equivalent to a delay through a register, the cited art clearly fails to teach or suggest delaying the input clock signal by an amount that is equal to the delay in the latching. Claim 14 is patentable over the cited art for similar reasons.

Rejection of Claims under 35 U.S.C. § 103

Claims 5, 8 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa, U.S. Patent No. 5,748,018, in view of Nichols, et al., U.S. Patent No. 6,356,557 B1). Applicant respectfully traverses these rejections for reasons similar to those provided above with respect to claim 1.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5080.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 20, 2004.

Brenna A Brock 2-20-2004

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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